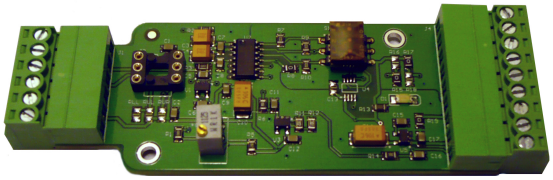
Embedded Strain Gauge and Load Cell Signal Conditioner/Amplifier

1 DESCRIPTION

The embedded strain gauge signal conditioner board is a low cost solution to your strain measurement needs. This miniaturized board accepts or completes a single Wheatstone bridge arranged in quarter, half, or full bridge configuration. In full bridge mode, it can also accept a standard load cell. Gain and offset adjustment can be controlled manually or programmably via standard SPI protocol. Easily interface with your microprocessor or ADC for reliable and low cost measurement of strain signals or any other application that requires a differential amplifier. Additionally, this board can be interfaced directly with any analog LabVIEW DAQ or other data acquisition system.

2 APPLICATIONS

- Strain gauge measurement
- Load cell measurement
- Bridge sensor amplifier
- Thermistor measurement
- General differential amplifier



3 FEATURES

- Optional 6 V - 16 V or 5 V only power supply options
- 5 V Bridge excitation
- Flexible on-board bridge completion resistor options (sold separately)
  - Through hole
  - Surface mount (0805 package)
  - Prototyping DIP socket (pluggable)
- Precision gain (0.1% tolerance typical)
- Calibration test results attached to each amplifier
- Manual or programmable gain: 110, 220, 550, 1100, 2200, 5500, 11000
- Gain can be customized at time of order 1/11 to 2 times gain range above
- Manual or programmable calibration offset
  - Manual: Potentiometer controlled
  - SPI controlled
- Noise elimination filters
  - Factory default low-pass: -3 dB at 180 Hz
  - Factory adjustable, per request
- Small profile (1.3” x 3.3”)

4 AVAILABLE OPTIONS

The EMBSGB can be configured with several options including manual or serial control as well as different style terminal blocks for the input and output signal headers. Please refer to the table below to determine the available configurations.

Table 1: Available Options

Model #	Gain Control		Offset Control		Connectors	
	Manual	SPI	Manual	SPI	Std*	OEM*
EMBSGB-M	X		X		X	
EMBSGB-S		X		X	X	
EMBSGB-MO	X		X			X
EMBSGB-SO		X		X		X

- (*) Standard versions feature pluggable terminal blocks on both ends of the amplifier. This version is shown above.
- (*) OEM versions feature unsoldered header pins to be configured by the user.
- Overall amplifier gain can be modified to users specifications (contact Tacuna Systems). Gain can be scaled 1/11(0.0909)-2 times the gain specified in the description or in Section **??**.

5 ELECTRICAL SPECIFICATIONS

The input and output electrical specifications for the EMBSGB are listed in the table below.

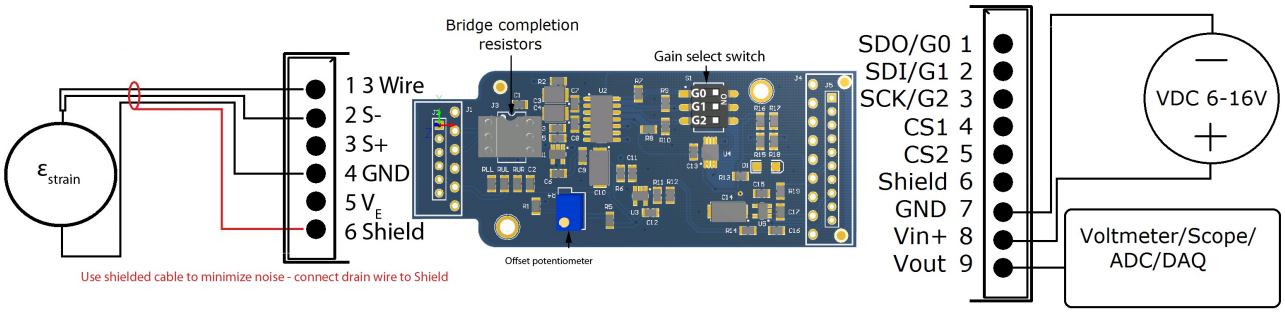
Table 2: Electrical Specifications

Parameter	Min	Typ	Max	Unit
Supply Voltage (DC)	6	9	16	V
SPI/logic low	-	-	1.5	V
SPI/logic high	3.5	-	-	V
Analog Out	0	-	5	V
Current (w/ 120 ohm bridge res)		52	100	mA

6 QUICKSTART

6.1 Manual quarter bridge

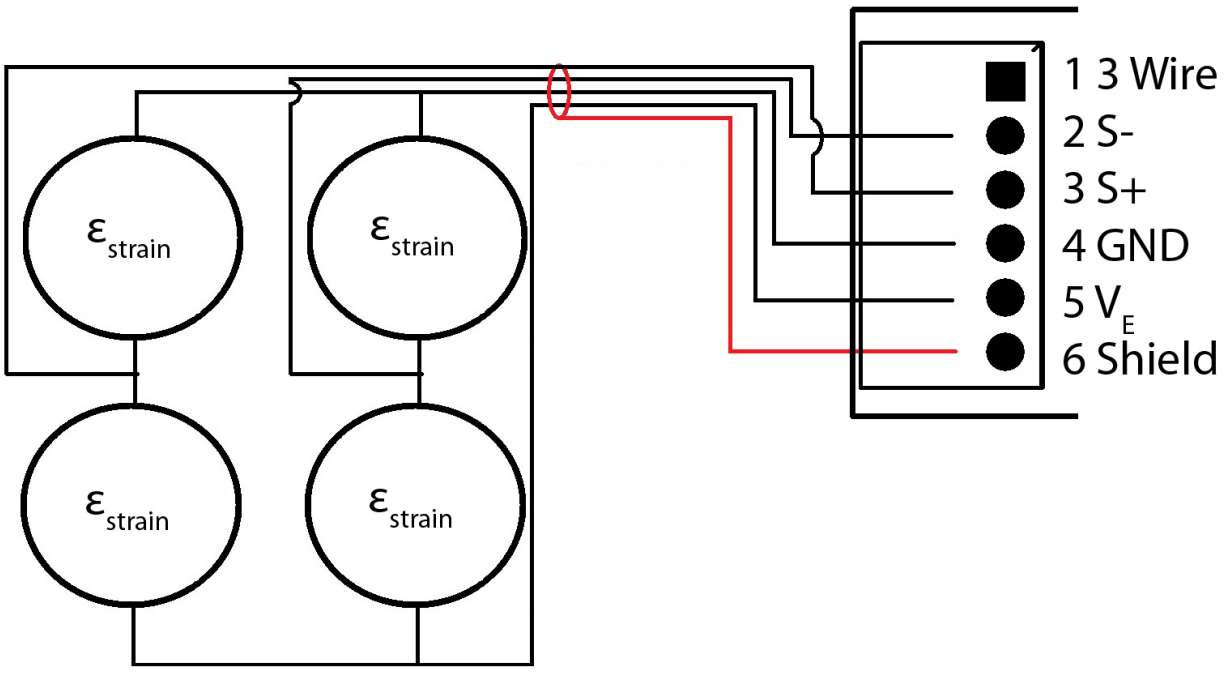
- Using ESD precautions, unpack and connect a strain gauge to the inputs of the EMBSGB (quarter bridge example seen below).
- Place correct value bridge completion resistors (if needed for non-quarter bridge).
- Apply a 6V to 16V DC power across pins 7 and 8 (Note the polarity). The green LED will indicate correct power to the system.
- Set the desired gain with the gain select switch as shown in Section **??**.
- Connect a voltmeter or other measurement device to the analog output pin 9.
- While reading the analog output with the system unloaded, adjust the potentiometer until the voltage reaches approximately 2.5V.
- Now the EMBSGB is properly set up and adjusted, you can now calculate strain from the output of the amplifier - see Section **??** for more information.



6.2 Manual full bridge/load cell

- Using ESD precautions, unpack and connect a strain gauge bridge or load cell to the inputs of the EMBSGB (full bridge/load cell example seen below).
- Apply a 6V to 16V DC power across pins 7 and 8 (Note the polarity). The green LED will indicate correct power to the system.
- Set the desired gain with the gain select switch as shown in Section **??**.
- Connect a voltmeter or other measurement device to the analog output pin 9.
- While reading the analog output with the system unloaded, adjust the potentiometer until the voltage reaches approximately 2.5V.

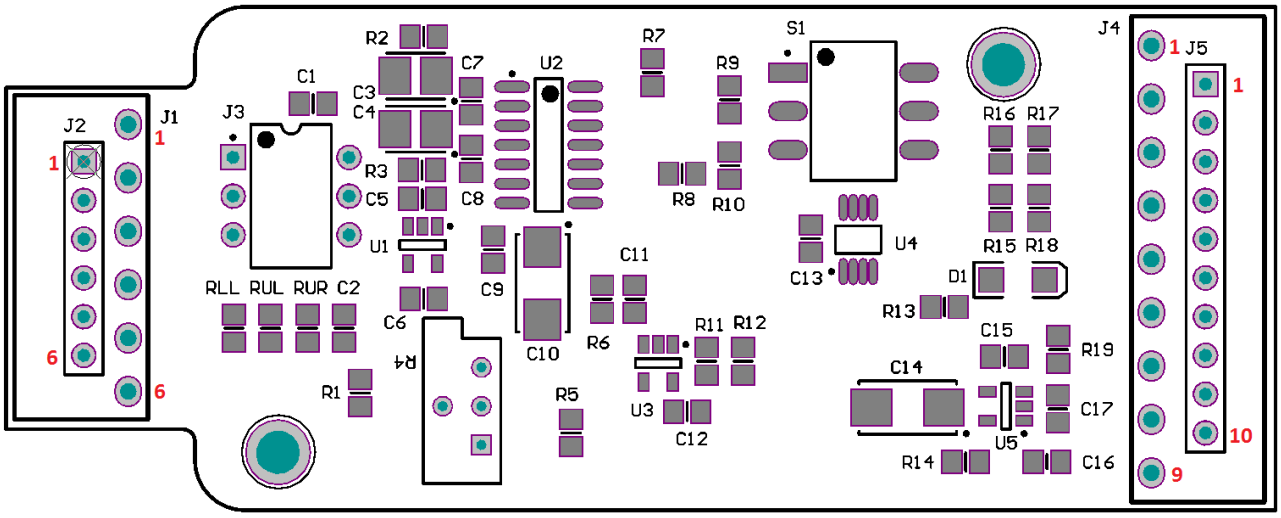
- Now the EMBSGB is properly set up and adjusted, you can now calculate strain from the output of the amplifier - see Section **??** for more information.



Use shielded cable to minimize noise - connect drain wire to Shield

No bridge completion resistors required

7 PINOUT



Input Signal Header

Headers J1 and J2 are used for connecting the strain gauge or load cell

Table 3: Pinout - Input Signal Header

Pin		Name	Description
J1:1	J2:1	3Wire	Third wire for quarter bridge config
J1:2	J2:2	S-	Negative sense
J1:3	J2:3	S+	Positive sense
J1:4	J2:4	GND	Ground
J1:5	J2:5	V_E	Excitation voltage or +5V supply
J1:6	J2:6	Shield	Connection for shielded cable drain

NOTE

The input signal header on Rev 1.2 boards is in reverse configuration from previous revisions. This was done so both headers would have Pin#1 on the same side of the board.

Output Signal Header

Headers J4 & J5 contain the output and control signals for the amplifier board

Table 4: Pinout - Output Signal Header

Pin		Name	Description	
			SPI Board	Manual Board
J4:1	J5:1	SDO/G0	Serial data out	NC
J4:2	J5:2	SDI/G1	Serial data in	NC
J4:3	J5:3	SCK/G2	Serial clock	NC
J4:4	J5:4	CS1	Cable select - Gain (PGA)	NC
J4:5	J5:5	CS2	Cable select - Offset (DAC)	NC
J4:6	J5:6	Shield	Connection for shielded wire	
J4:7	J5:7	GND	Ground supply voltage	
J4:8	J5:8	Vin+	Positive supply voltage +6.0 V to +16.0 V	
J4:9	J5:9	Vout	Analog voltage output	
–:–	J5:10	+5V	Optional +5Vin - Use with regulated +5V supply (use only when not supplying Vin)	

NOTE

Digital offset control available on EMBSGB-S# only.

8 BLOCK DIAGRAM

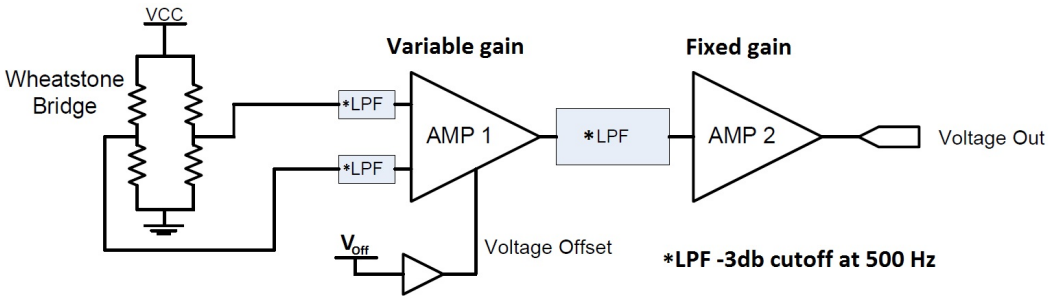
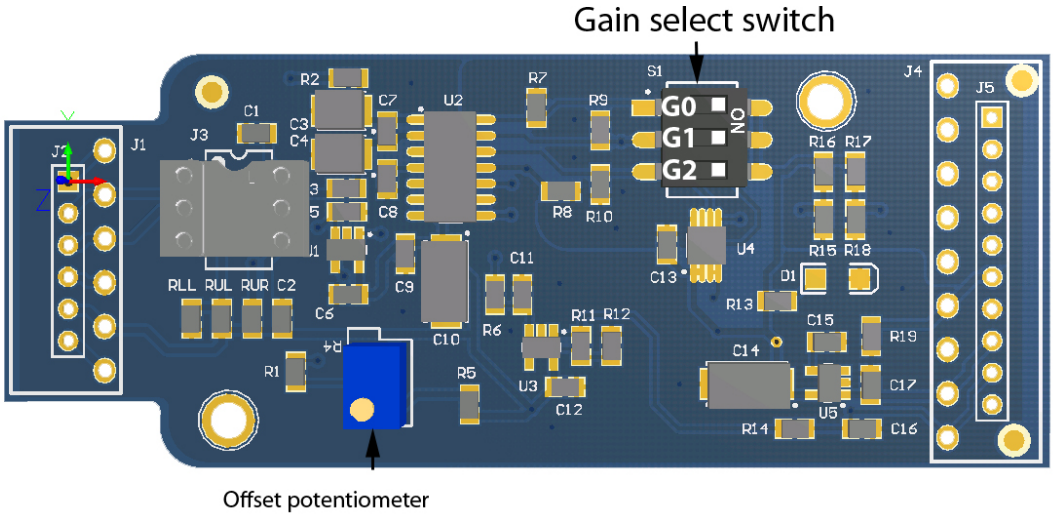


Figure 8.1: Amplification Stage

*Low pass filter default is 180 Hz, but can be customized to the desired corner frequency.

9 MANUAL CONTROL

In the manual version, gain is controlled by the three gain control switches and the offset is controlled through the offset adjustment potentiometer.



9.1 MANUAL GAIN CONTROL

The gain of the second stage amplifier is fixed at 11. However, the gain of the primary stage amplifier can be controlled by the three gain control DIP switches. The total gain of the amplifier board is calculated by multiplying the gain of the two amplifiers together. The *total gain* of the amplifier board is listed in the following table.

G2 (MSB)	G1	G0 (LSB)	Total Gain (G_{AMP1}*G_{AMP2})
OFF	OFF	OFF	110
OFF	OFF	ON	220
OFF	ON	OFF	550
OFF	ON	ON	1100
ON	OFF	OFF	2200*
ON	OFF	ON	5500*
ON	ON	OFF	11000*
ON	ON	ON	DO NOT USE

*Gains above 1000 are not recommended without careful consideration of noise and might require additional shunt resistors to prevent the first stage amplifier from saturating.

9.2 MANUAL OFFSET CONTROL

For most applications, use the offset potentiometer to adjust the output voltage to near the middle of the range for V_{out} (Approx 2.5 V). Adjusting the output voltage to 2.5 V allows for maximum range of both positive and negative strain. If your strain gauge is known to only flex in one direction, you may find it more useful to adjust the output voltage closer to the top or bottom of the V_{out} range so you can get maximum resolution from your ADC.

NOTE

The offset potentiometer will need to be readjusted for each gain alteration and/or bridge configuration.

10 PROGRAMMABLE CONTROL

In the programmable version, gain, offset, and other features are controlled via a standard SPI serial stream.

10.1 PROGRAMMABLE GAIN CONTROL

Programmable gain control is made available from the LMP8358 instrumentation amplifier from National Semiconductor http://www.national.com/ds/LM/LMP8358.pdf. Excerpts are taken directly from National Semiconductor.

Serial Control Interface Operation

The LMP8358 gain, bandwidth compensation, shutdown, input options, and fault detection are controlled by an on board programmable register. Data to be written into the control register is first loaded into the LMP8358 via the serial interface. The serial interface employs an 16-bit double-buffered register for glitch-free transitions between settings. Data is loaded through the serial data input, SDI. Data passing through the shift register is output through the serial data output, SDO. The serial clock, SCK controls the serial loading process. All sixteen data bits are required to correctly program the amplifier. The falling edge of CSB enables the shift register to receive data. The SCK signal must be high during the falling and rising edge of CSB. Each data bit is clocked into the shift register on the rising edge of SCK. Data is transferred from the shift register to the holding register on the rising edge of CSB. Operation is shown in the SPI Timing Diagram. The serial control pins can be connected in one of two ways when two or more LMP8358s are used in an application.

10.1.1 Control Register

Bit #	Name	Description
0	G0	Gain setting (LSB)
1	G1	Gain setting
2	G2	Gain setting (MSB)
3	COMP0	Frequency compensation setting (LSB)
4	COMP1	Frequency compensation setting
5	COMP2	Frequency compensation setting (MSB)
6	MUX0	Input multiplexer selection (LSB)
7	MUX1	Input multiplexer selection (MSB)
8	POL	Input polarity switch
9	SHDN	Shutdown Enable
10	FILT	Do not use, set to 0
11	PIN	Do not use, set to 0
12	CUR0	Do not use, set to 0
13	CUR1	Do not use, set to 0
14	CUR2	Do not use, set to 0
15	N/A	Unused, set to 0

10.1.2 Gain Control (Register bits 0:2)

The three gain control bits allow for the selection of seven different gains.

G2 (MSB)	G1	G0 (LSB)	Total gain
0	0	0	110
0	0	1	220
0	1	0	550
0	1	1	1100
1	0	0	2200*
1	0	1	5500*
1	1	0	11000*
1	1	1	DO NOT USE

*Gains above 1000 are not recommended without careful consideration of noise, and might require additional shunt resistors to prevent the first stage amplifier from saturating.

10.1.3 Frequency Compensation (Register bits 3:5)

The gain-bandwidth compensation is set to one of five levels under program control. The amount of compensation can be decreased to maximize the available bandwidth as the gain of the amplifier is increased. The compensation level is selected by setting bits COMP[2:0] of the control register with 000b, 001b, 010b, 011b, or 1xxb. Frequency Compensation (Register bits 5:3) shows the bandwidths achieved at the selectable gain and compensation settings. Note that for gains 110X and 220X, the recommended compensation setting is 000b. For the gain setting 550X, compensation settings may be 000b and 001b. Gain settings 1100X and 2200X may use the three bandwidth compensation settings 000b, 001b, and 010b. At gains of 5500X and 11000X, all bandwidth compensation ranges may be used. Note that for lower gains, it is possible to under compensate the amplifier into instability.

	Bandwidth Frequency Compensation				
Gain	000	001	010	011	1xx
110	930 kHz	n/a	n/a	n/a	74 kHz
220	385 kHz	n/a	n/a	n/a	37 kHz
550	160 kHz	460 kHz	n/a	n/a	16 kHz
1100	80 kHz	225 kHz	640 kHz	n/a	8 kHz
2200	38 kHz	95 kHz	195 kHz	n/a	4 kHz
5500	16 kHz	40 kHz	85 kHz	130 kHz	1.5 kHz
11000	8 kHz	22 kHz	50 kHz	89 kHz	0.8 kHz

10.1.4 Input Multiplexer and Polarity Switch (Register bits 6:8)

The input multiplexer allows for additional control in many situations that will not be used and should therefore be fixed to 0,0. The polarity switch can reverse the input polarity from

the Wheatstone bridge to the input of the first stage amplifier, this can be useful for high gain situations if the minimum offset compensation has pushed the output voltage beyond the desired operating region. This can also be useful to quickly change the sign of strain measurement.

MUX0 (LSB)	MUX1 (MSB)	POL	Description
0	0	0	Normal polarity, S+ to pos input & S- to neg input of amplifier (*Recommended)
0	0	1	Reverse polarity, S- to pos input & S+ to neg input of amplifier
0	1	x	DO NOT USE
1	0	x	DO NOT USE
1	1	x	DO NOT USE

10.1.5 Shutdown Enable (Register bit 9)

When the SHDN bit of the LMP8358 register is set to 1b the part is put into shutdown mode.

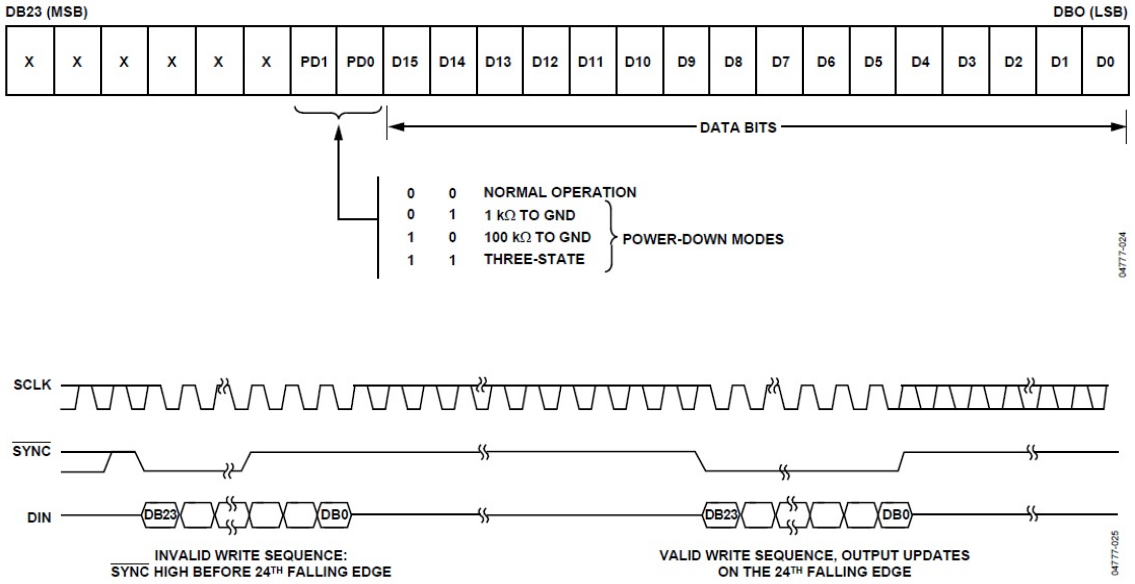
SHDN	Mode
0	Active mode
1	Shutdown mode

10.2 PROGRAMMABLE OFFSET CONTROL

Programmable offset control is made available from a 16 bit digital to analog converter, the AD5662 from Analog Devices http://www.analog.com/static/imported-files/data_sheets/AD5662.pdf. Excerpts are taken directly from analog devices.

10.2.1 Serial Control

The write sequence begins by bringing the CS line low. Data from the SDI line is clocked into the 24-bit shift register on the falling edge of SCK. The serial clock frequency can be as high as 30 MHz, making the AD5662 compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the CS line can be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of CS can initiate the next write sequence. Since the CS buffer draws more current when VIN = 2.4 V than it does when VIN = 0.8 V, CS should be idled low between write sequences for even lower power operation. As mentioned previously it must, however, be brought high again just before the next write sequence.



The output voltage from the DAC will depend on the 16 bit number passed into the register. In decimal form the number can range from 0 to 65,536. Representing a range from 0 to 5V. The output voltage can be calculated below.

$$V_O = 5\frac{D}{65,536}V \tag{1}$$

10.2.2 Power Down Modes

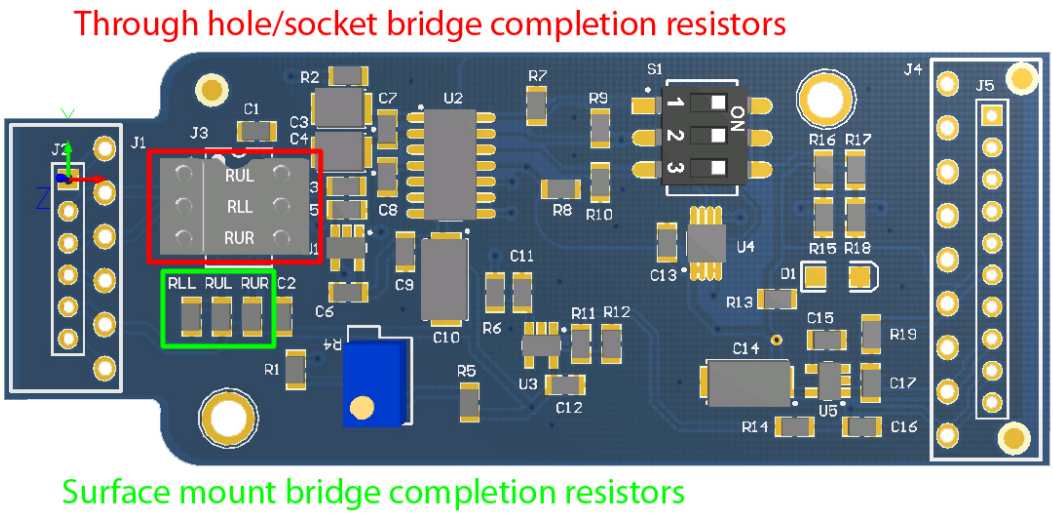
The AD5662 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB17 and DB16) in the control register. Below is the state of the bits corresponds to the devices mode of operation.

DB17	DB17	Operating Mode
0	0	Normal Operation
0	1	Power-Down (1 kΩ to GND)
1	0	Power-Down (100 kΩ to GND)
1	1	Power-Down (Open/floating)

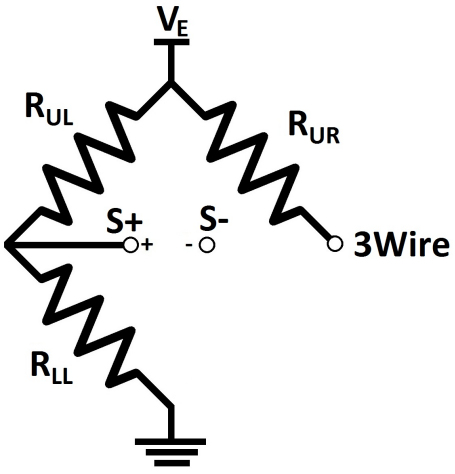
When both bits are set to 0, the part works normally with its normal power consumption of 250 μA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ or 100 kΩ resistor, or left open-circuited.

11 BRIDGE CONFIGURATION

The bridge can be configured in many ways and can be completed by on board bridge completion resistors. To complete the bridge you can use 0805 surface mount resistors or standard through hole resistors placed in the DIP socket shown in the board diagram.



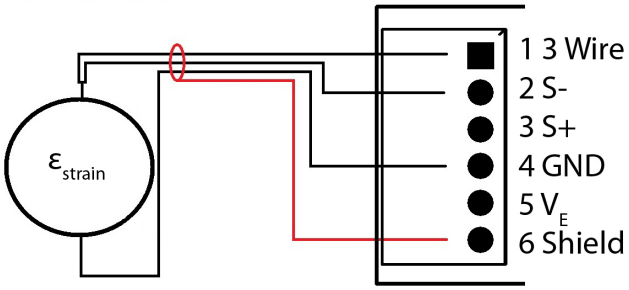
The simplified schematic of the bridge completion circuit is shown below, the two types of resistors (surface mount and through hole are wired in parallel).



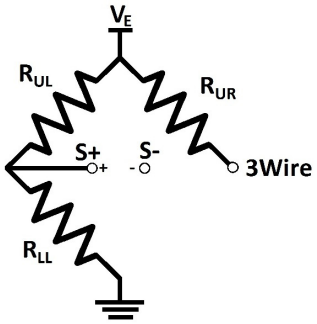
Shielded wire should be used to minimize EM noise.

11.1 Quarter Bridge

Quarter bridge utilizes the three wire configuration to minimize the effect of wire resistance. In addition all three bridge completion resistors are required.



Use shielded cable to minimize noise - connect drain wire to Shield

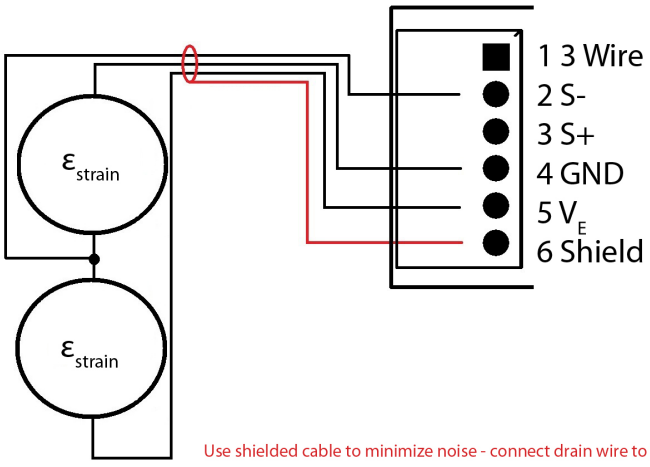


Connect three bridge completion resistors

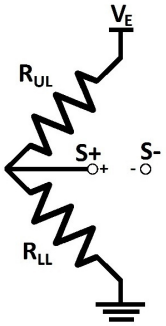
$$V_{\text{S, quarter}} = \frac{V_E G F \epsilon}{4} \tag{2}$$

11.2 Half Bridge

Half bridge only uses the two left side bridge completion resistors.



Use shielded cable to minimize noise - connect drain wire to Shield

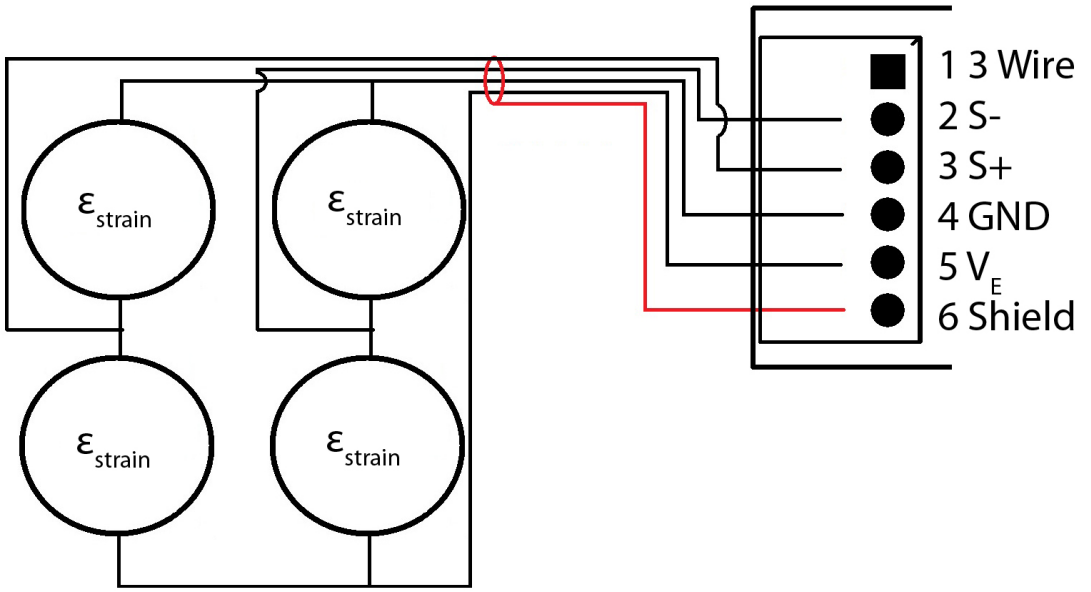


Connect left two bridge completion resistors

$$V_{\text{S, half}} = \frac{V_E G F \epsilon}{2} \tag{3}$$

11.3 Full Bridge

A load cell or a full bridge require no completion resistors.



$$V_{\mathrm{S,\ half}} = V_E G F \epsilon \tag{4}$$

12 STRAIN AND GAIN ACCURACY

Parameter	Min	Typ	Max	Unit
1st stage amp. gain error		0.03	0.15	%
2nd stage amp. gain error		0.02	0.1	%

13 TROUBLSHOOTING

No LED power indication

Check connections, the power plug is the large connector. With the large connector on the right and the small connector on the left (component side up) the pins count increasingly from top to bottom.
Check power requirements, the supply voltage requires a minimum voltage of 6 V and a maximum of 16V along with a maximum of 100 mA of current.

Saturated low or high output signal

Saturated high

Check that wheatstone bridge is well balanced, if not use shunting resistors to correct any errors.
Check if amplification gain is too high, using correct MSB to LSB orientation.
Progressively high gain requires a further balanced wheatstone to prevent saturation.

Check if potentiometer (Manual mode) or DAC (SPI) reference voltage is too high.

Check connections, the gauge input/load connects to the small connector. With the large connector on the right and the small connector on the left (component side up) the pins count increasingly from top to bottom.

Saturated low

Check that wheatstone bridge is well balanced, if not use shunting resistors to correct any errors.
Check if amplification gain is correct, using correct MSB to LSB orientation.
Progressively high gain requires a further balanced wheatstone to prevent saturation at low or high rails.

Check if potentiometer (Manual mode) or DAC (SPI) reference voltage is too low.

Check connections, the gauge input/load connects to the small connector. With the large connector on the right and the small connector on the left (component side up) the pins count increasingly from top to bottom.

14 NOTES